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(54) **Pager Decoding System with Intelligent Synchronisation Circuit**

(57) A portable addressable radio paging unit, capable of detecting and storing up to four different alerting signals per user, is responsive to a transmission signal including a preamble (100) to enable bit-synchronisation, a recurring synchronisation code word (101), and one or more address code words (102) within a batch (103) of code words transmitted between each synchronisation code word and the next. After achieving bit synchronisation, the receiver attempts word synchronisation using the next synchronisation code word (101). If this fails, at least one further attempt at word synchronisation is made, using subsequent word(s) (101). If failure persists, bit-synchronisation is returned to. Only one predetermined pair (i.e. one frame) of address code words in a batch can relate to the particular receiver, so after word synchronisation, battery is saved by switching off for the rest of the batch except that frame.

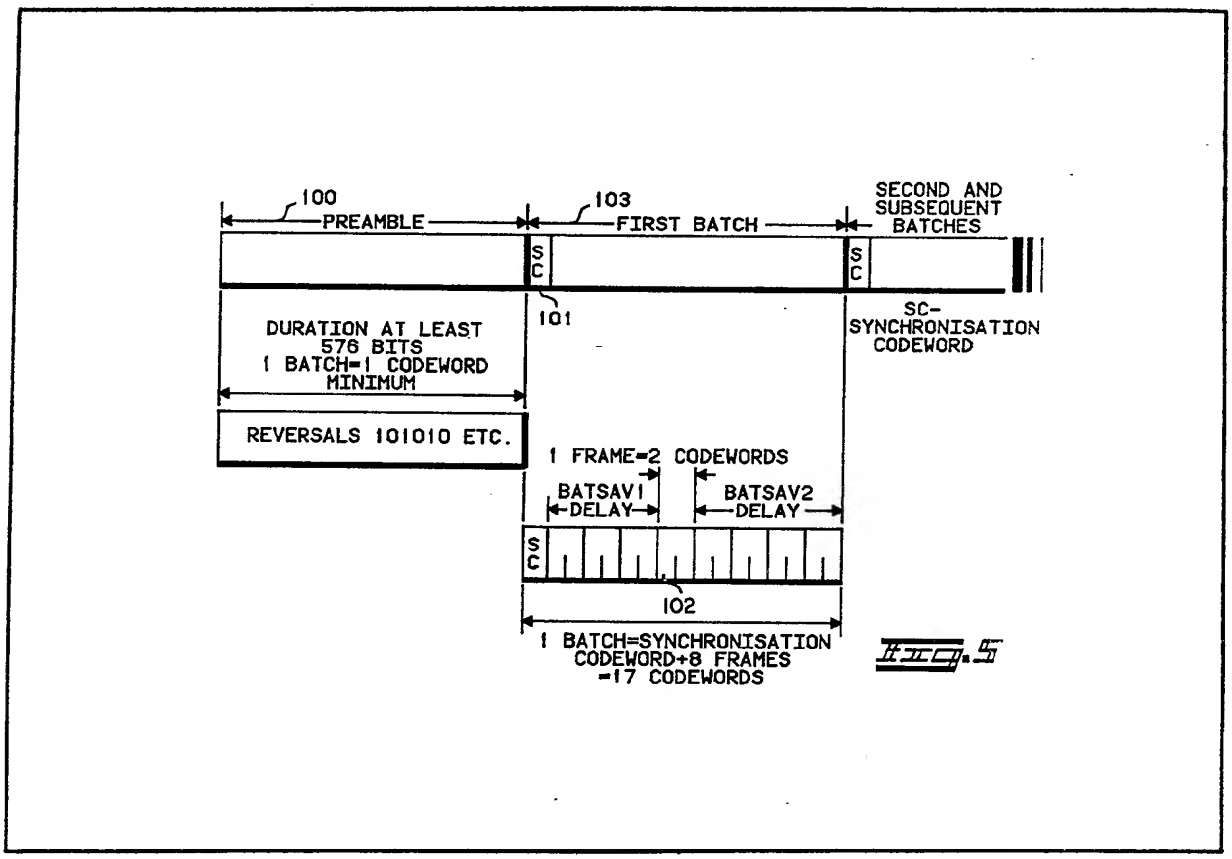

Fig. 5

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The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

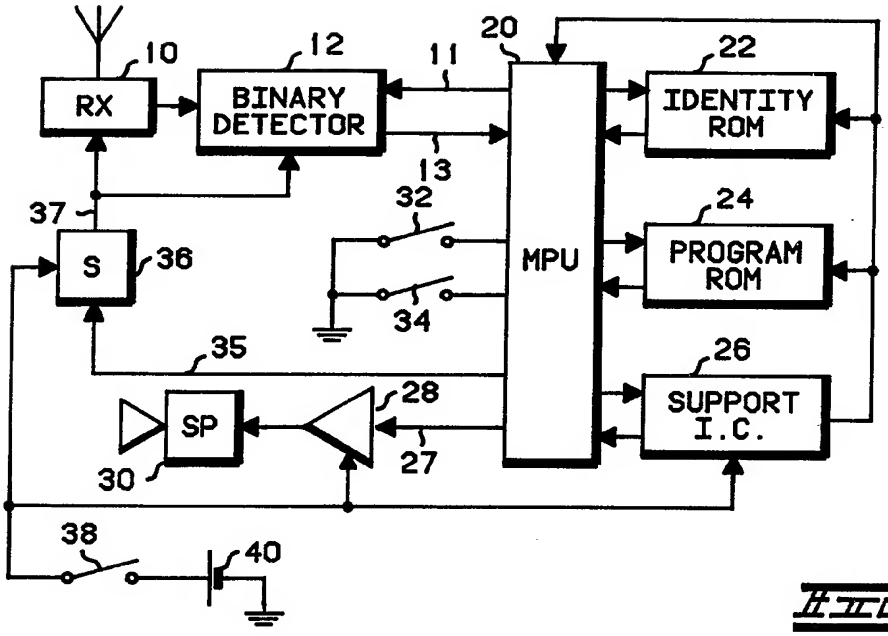

RX
10
BINARY DETECTOR
12
11
20
22
IDENTITY ROM
13
37
32
24
S
36
MPU
PROGRAM ROM
34
35
26
SUPPORT I.C.
28
SP
27
30
38
40

Fig.1

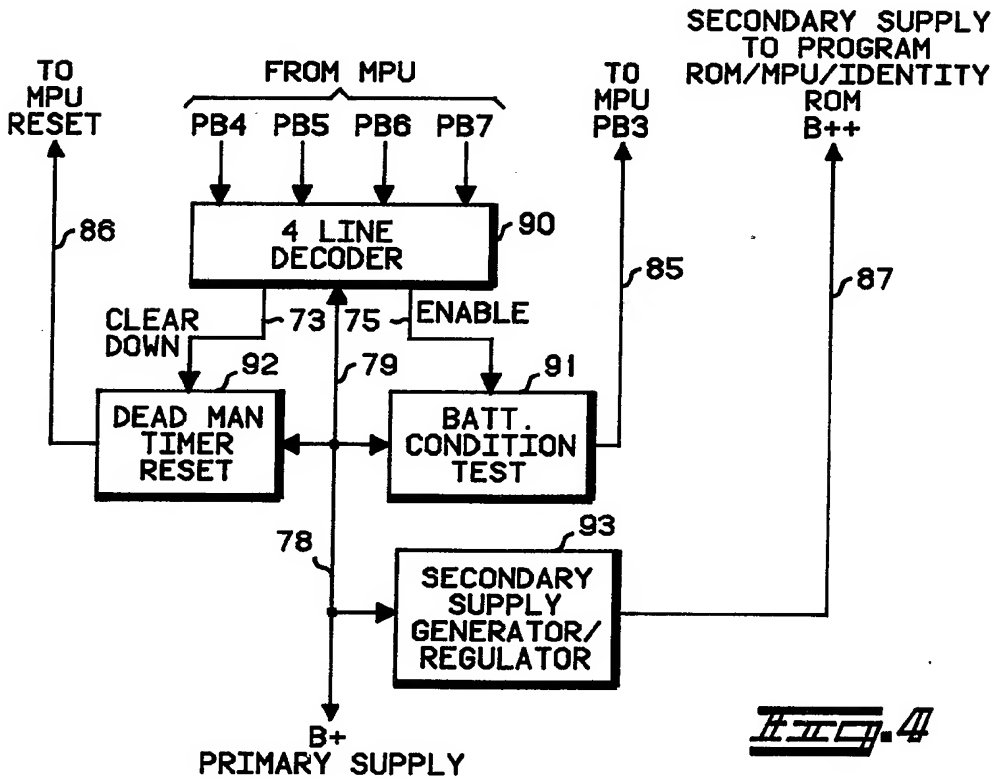
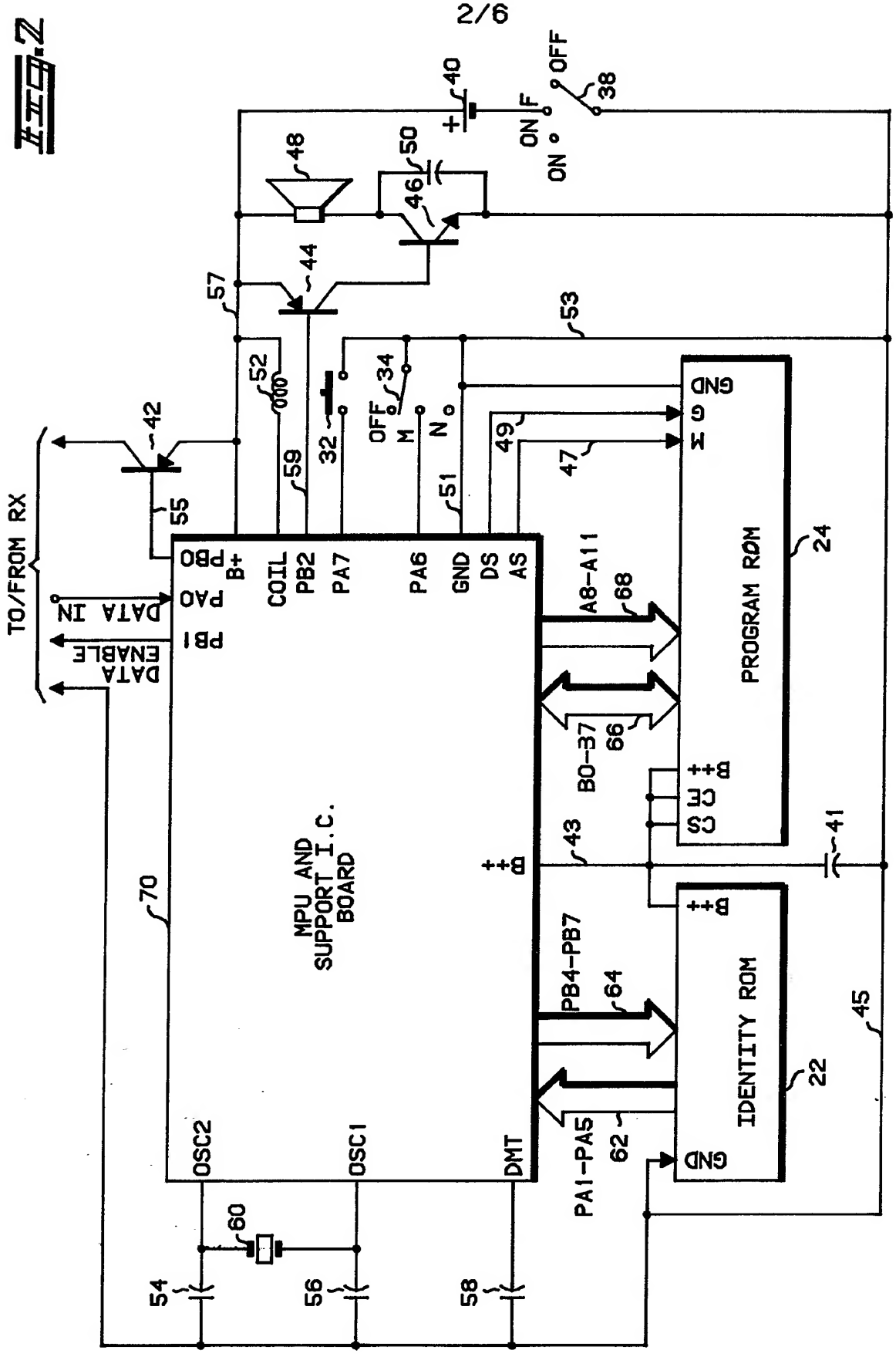

TO MPU RESET
FROM MPU
PB4 PB5 PB6 PB7
TO MPU PB3
SECONDARY SUPPLY TO PROGRAM ROM/MPU/IDENTITY ROM B++
86
4 LINE DECODER
90
85
87
CLEAR DOWN
73
75
ENABLE
92
79
91
DEAD MAN TIMER RESET
BATT. CONDITION TEST
78
93
SECONDARY SUPPLY GENERATOR/ REGULATOR
B+ PRIMARY SUPPLY

Fig.4

FIG.2


TO/FROM RX
DATA IN
DATA ENABLE
PB0
PA0
PB1
B+
COIL
PB2
PA7
PA6
GND
DS
AS
A8-A11
B0-37
PROGRAM ROM
24
GND
G
M
49
47
51
59
32
52
OFF
M
N
34
42
55
57
44
48
50
46
40
+
ON
OFF
38
53
MPU AND SUPPORT I.C. BOARD
70
B++
43
41
CS
CE
B++
PB4-PB7
64
IDENTITY ROM
22
45
PA1-PA5
62
GND
OSC2
OSC1
DMT
60
54
56
58

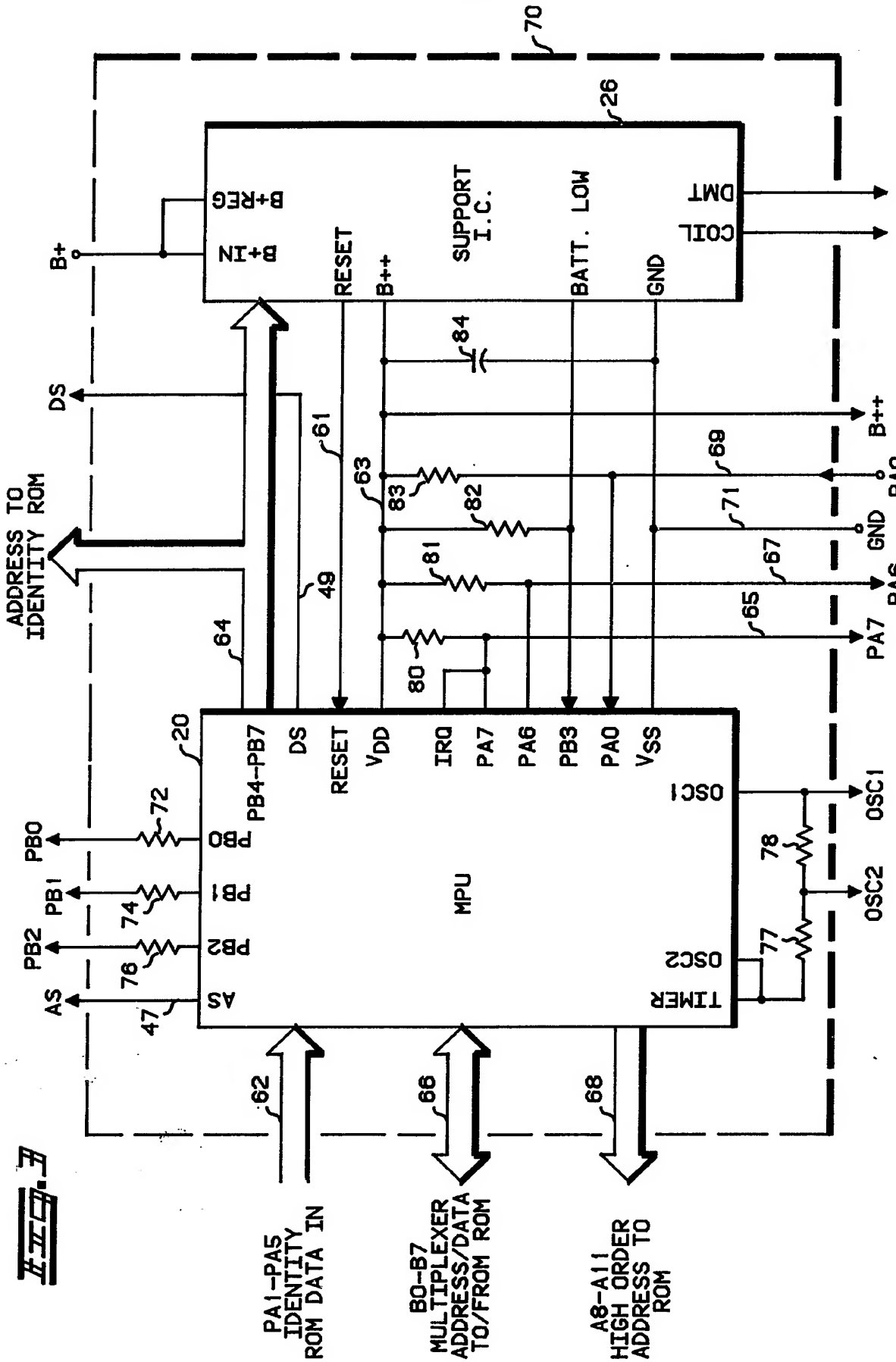

70
26
B+REG
B+IN
B+
RESET
B++
SUPPORT I.C.
BATT. LOW
GND
DMT
COIL
84
DS
61
63
83
82
81
80
64
49
69
71
67
65
B++
PA0
GND
PA6
PA7
ADDRESS TO IDENTITY ROM
20
PB4-PB7
DS
RESET
VDD
IRQ
PA7
PA6
PB3
PA0
VSS
OSC1
72
PB0
PB1
PB2
AS
74
76
47
MPU
78
77
OSC2
TIMER
62
66
68
PA1-PA5 IDENTITY ROM DATA IN
B0-B7 MULTIPLEXER ADDRESS/DATA TO/FROM ROM
A8-A11 HIGH ORDER ADDRESS TO ROM

FIG. 3

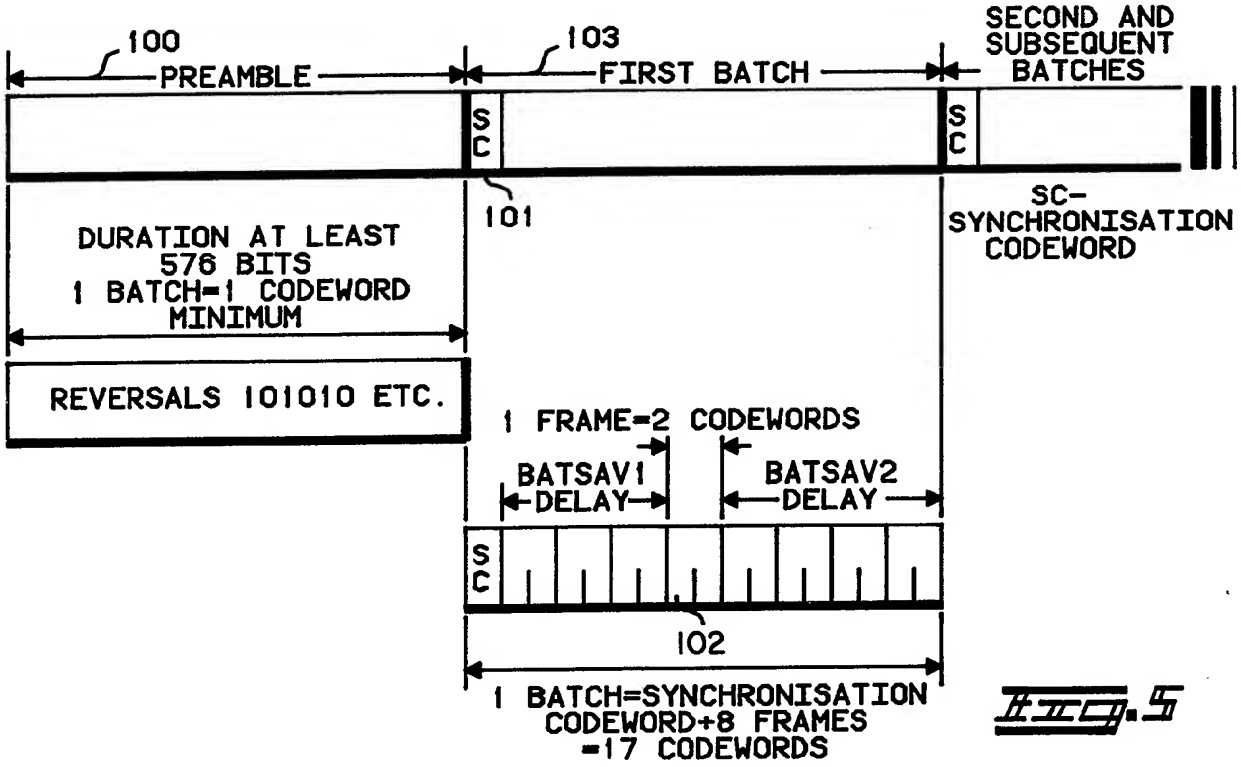


Fig.5

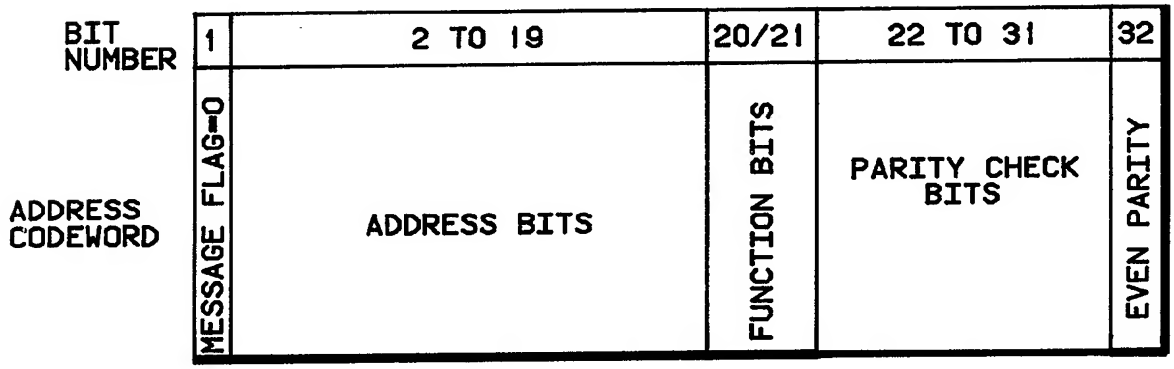
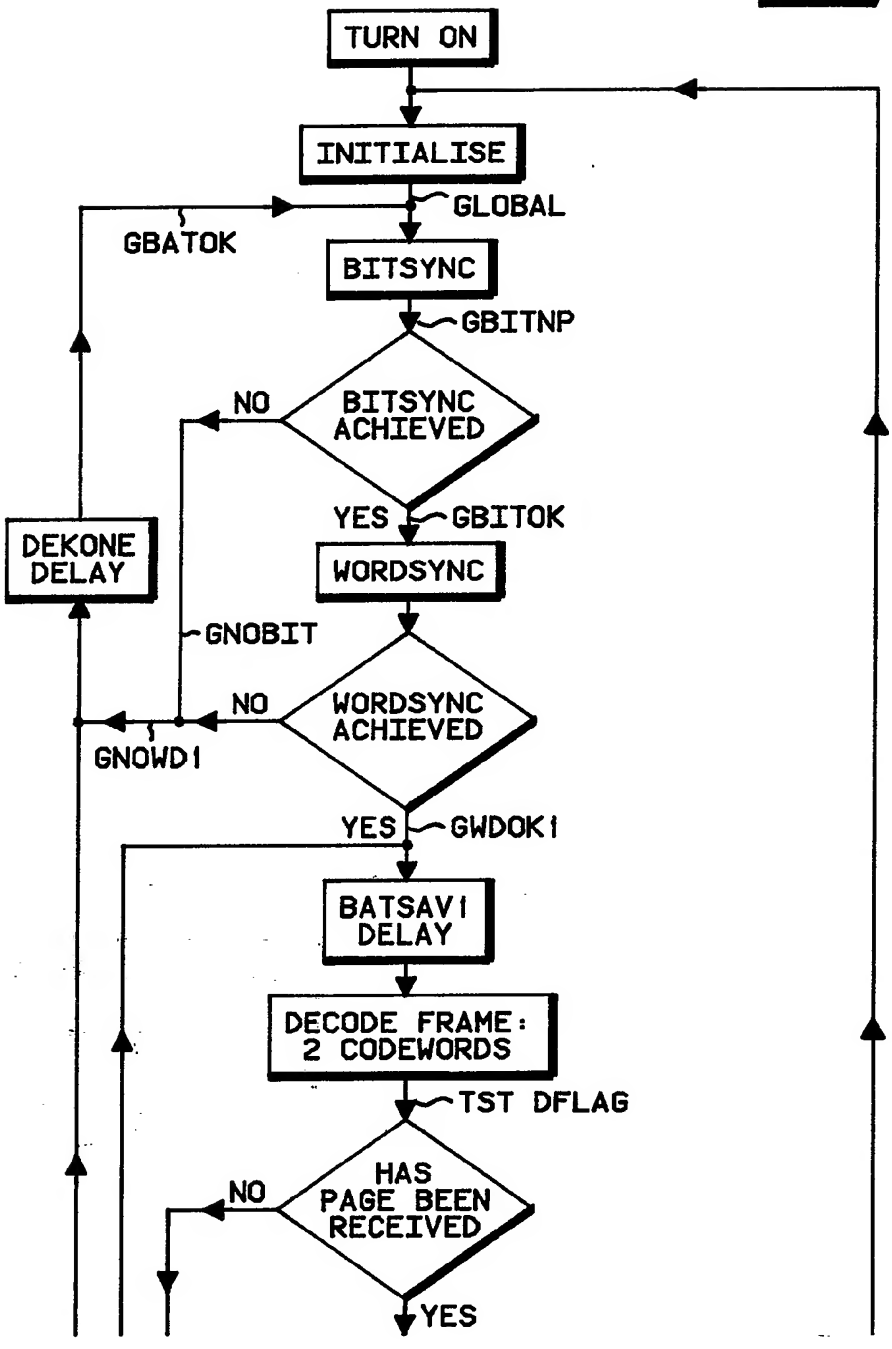


Fig.6

BIT NO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BIT	0	1	1	1	1	1	0	0	1	1	0	1	0	0	1	0
BIT NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
BIT	0	0	0	1	0	1	0	1	1	1	0	1	1	0	0	0

Fig.7

FIG. 9A


TURN ON
INITIALISE
GLOBAL
GBATOK
BITSYNC
GBITNP
NO
BITSYNC ACHIEVED
YES
GBITOK
DEKONE DELAY
WORDSYNC
GNOBIT
NO
WORDSYNC ACHIEVED
GNOWD1
YES
GWDOK1
BATSAV1 DELAY
DECODE FRAME: 2 CODEWORDS
TST DFLAG
NO
HAS PAGE BEEN RECEIVED
YES

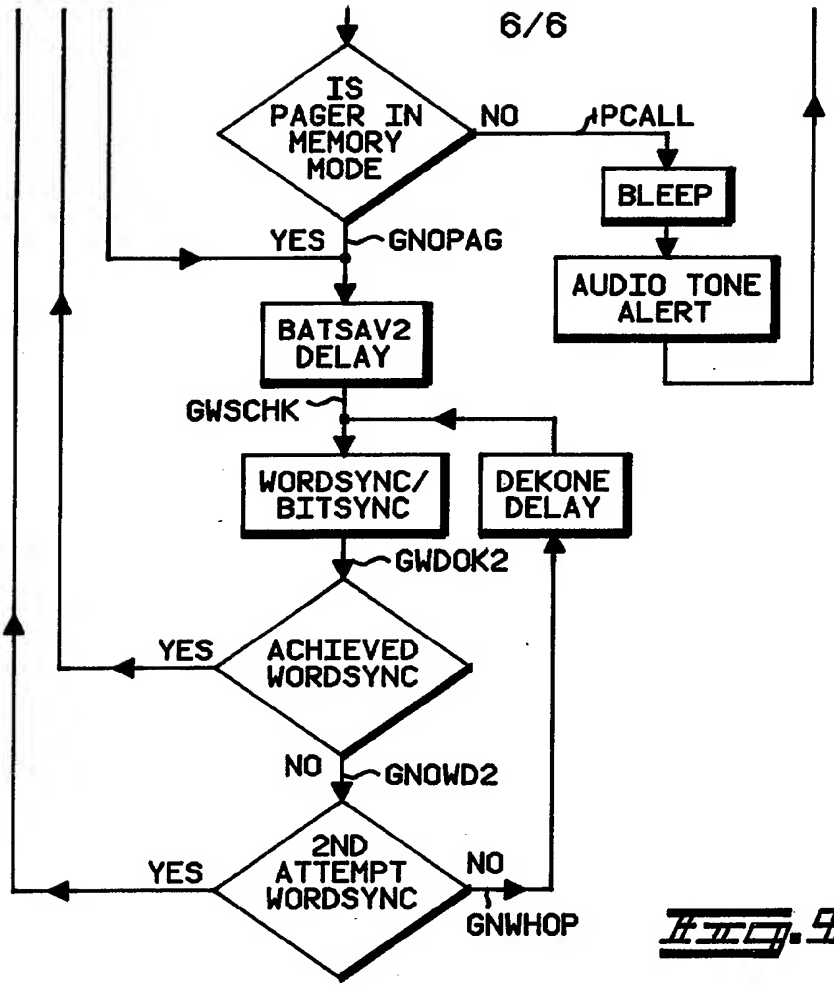


Fig. 9B

BIT NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BIT	0	1	1	1	1	0	1	0	1	0	0	0	1	0	0	1
BIT NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
BIT	1	1	0	0	0	0	0	1	1	0	0	1	0	1	1	1

Fig. 8

SPECIFICATION

Pager Decoding System with Intelligent Synchronisation Circuit

Related Invention

1. Microcomputer with Branch on Bit Set/Clear Instructions, invented by J. F. Boney, E. J. Rupp, II, and J. S. Thomas, U.S. Ser. No. 035,138, filed May 1, 1979, and assigned to Motorola Inc.

Technical Field

This invention relates generally to portable radio paging devices, and, in particular, to a decoding system having an intelligent synchronisation circuit for improving the efficiency and sensitivity of the paging device.

Background Art

The present invention concerns a decoding circuit for incorporation in a radio paging receiver and user notification unit which has been designed to operate with paging systems employing the standardised code established by the British Post Office Code Standardisation Advisory Group (POCSAG). The POCSAG transmission protocol is summarised in the document entitled "A Standard Code for Radio Paging" published by the British Post Office in June 1978. While details of the POCSAG standardised code and paging system are provided by the aforementioned document, a brief summary of the POCSAG transmission protocol will enable a better understanding of the present invention.

The POCSAG standardised code is designed for a large capacity, wide-area radio paging system. The specific code is a direct frequency shift keying (FSK) digital code which is transmitted at a bit rate of 512 bits per second. Fig. 5 gives the signal format, which comprises a preamble of alternate ones and zeros followed by one or more batches. Each batch comprises a 32-bit synchronisation code word followed by eight frames, each comprising a pair of 32-bit code words. As the POCSAG paging system is currently implemented each pair of code words in a frame may be assumed to be address code words. The transmission ceases when there are no further calls to be made and is re-instituted by the transmission of a new preamble. The transmission of the preamble permits the pagers to attain bit synchronisation in preparation for acquiring word synchronisation.

As mentioned above, the code words are transmitted in batches each of which comprises a synchronisation code word followed by eight frames each containing two code words. The frames are numbered zero to seven, and the pager population is similarly divided into eight groups. Each pager is assigned one of the eight frames according to the three least significant bits of its 21 bit identity, and it will only examine address code words in that frame.

Fig. 6 illustrates the address code word format. Bit 1 of the address code word is always zero. Bits 2—19 are address bits corresponding to the 18 most significant bits of the 21 bit pager identity. The three least significant bits are not transmitted but serve to define the frame in which the address code word(s) must be transmitted.

Bits 20 and 21 of the address code word are the two function bits which are used to select the required address from the four assigned to the pager, enabling each pager to respond to a total of four types of alerting signals. Bits 22—31 are the check bits generated by a Bose-Chaudhuri-Hocquenghen (BCH) block code polynomial, and bit 32 is chosen to provide even parity.

Fig. 7 illustrates the synchronisation code word, which is always of the value shown. Fig. 8 illustrates the idle code word, also always of the value shown, which is transmitted whenever an address code word is not transmitted within a frame.

The POCSAG standardised code thus requires that the pager decoding circuit first achieve bit synchronisation in response to the preamble portion of the transmission and then achieve word synchronisation in response to the synchronisation code word. Once word synchronisation is achieved, the decoding circuit has a time reference with which to synchronise itself to the relative position of its assigned frame within each transmitted batch of frames containing address code words. For example, a pager assigned to receive address code words in the third frame of each batch will be able to synchronise itself to decode the address code words transmitted in the third frame of each transmitted batch to see whether it is receiving a page specifically directed to it.

In the normal operation of the decoding circuit, therefore, it would perhaps be the most apparent procedure to first attempt to achieve synchronisation to the preamble bits, and then attempt synchronisation to the synchronisation code word. Once word synchronisation were achieved, the decoder would look at the address information in the specific frame location assigned to it in each batch. However, if word synchronisation were not achieved for any reason, the most obvious procedure would be to immediately re-attempt bit synchronisation as a pre-condition to any further attempt to achieve word synchronisation.

The decoding circuit of the present invention, on the other hand, employs a synchronisation strategy which tolerates at least some degree of error in the attempt to achieve word synchronisation, the ultimate result being a decoder which is more sensitive (i.e. has a higher success rate) than would otherwise be achieved. The decoding circuit of the present invention includes means for examining the transmitted bit pattern to search for the presence of the synchronisation code word. When a match, or

a near-match, to the synchronisation code word is achieved, the decoding circuit is deemed to be in word synchronisation. It then evaluates the address information in its respective assigned frame to see whether it has received a paging request.

However, if the match between a received synchronisation code word and the stored reference synchronisation code word exceeds a pre-determined number of bit errors, the decoding circuit ignores the informational content of its respective frame, and it makes a second attempt at word synchronisation by trying to synchronise with the synchronisation code word of the subsequent batch. If synchronisation is achieved with the synchronisation code word of the subsequent batch, within the pre-determined margin of error, word synchronisation is considered to have been achieved. However, if, after a second attempt at word synchronisation, no synchronisation is achieved, the operation of the decoding circuit is returned to the bit synchronisation operation.

The advantage of the intelligence built into the decoding circuit of the present invention is that in a decoding system in which a finite amount of time is required to achieve bit synchronisation, any automatic reversion to the bit synchronisation operation after a first failure at word synchronisation would result in the possible loss of paging information. The intelligent synchronisation circuit of the present invention acknowledges the fact that an initial failure to synchronise on the synchronisation code word may result from a noise burst or transmission fade occurring during the transmission of the synchronisation code word, which disturbance should not necessarily be permitted to cause the synchronisation circuit to revert to the bit synchronisation operation, with the resultant possible loss of paging information.

By permitting a second attempt at word synchronisation, the present invention acknowledges the possibility that the failed word synchronisation operation would have been successful but for a momentary reception fault. As a result, pagers employing the intelligent synchronisation circuit of the present invention have a higher probability of receiving the paging information intended for them.

The present invention also incorporates a battery saving feature in that the power supply to various of the system components is cut during the time periods of the transmission when the informational content of the transmission is of no interest to the pager. Thus the decoding circuit includes means for calculating the time delay between the end of the synchronisation code word and the beginning of the frame assigned to the particular pager, and it cuts the power supply during this period. In addition, the power supply is cut during the time period between the end of the frame assigned to the particular pager and the beginning of the subsequent synchronisation code word. In this manner the drain on the pager battery is substantially reduced, thus providing substantially improved battery life and user convenience.

Brief Summary of Invention

It is therefore an object of the present invention to provide an improved decoding system within the context of a radio pager, which decoding system is provided with an intelligent synchronisation circuit which makes one or more repeated attempts at achieving word synchronisation, so that the word synchronisation status is not unnecessarily lost, thus reducing the chance that paging information will be lost.

It is also an object of the present invention to provide a decoding system which includes a battery conserving feature.

These and other objects are achieved in accordance with a preferred embodiment of the invention by providing a decoding system for use with a receiver receiving a transmission signal comprising a periodically recurring synchronisation code word and at least one address code word such decoding system comprising means for receiving the synchronisation code word, means for comparing a received synchronisation code word with a reference code word and for generating an indication of the quality of the received synchronisation code word, means for generating a comparison count representative of the number of successive comparisons of successively received synchronisation code words with the reference code word, and decisional means responsive to the quality indication and to the comparison count, the decisional means generating a first signal if the quality of a received synchronisation code word exceeds a predetermined threshold value, generating a second signal if the quality of the received synchronisation code word does not exceed a pre-determined threshold value and a pre-determined number of comparison counts has not been exceeded, and generating a third signal if the quality of the received synchronisation code word does not exceed the pre-determined threshold value and the pre-determined number of comparison counts has been exceeded.

Brief Description of Drawings

The invention is pointed out with particularity in the appended claims. However, other features of the invention will become more apparent and the invention will be best understood by referring to the following detailed description in conjunction with the accompanying drawings in which:

Fig. 1 shows a block diagram illustrating a preferred embodiment of a pager incorporating the decoding system of the present invention.

Fig. 2 shows a block diagram illustrating the decoding system of the present invention.

Fig. 3 shows a circuit schematic of the MPU and support I.C. shown in Fig. 2.
Fig. 4 shows a more detailed block diagram of the support I.C. shown in Fig. 3.
Fig. 5 illustrates the POCSAG signal transmission format.
Fig. 6 illustrates the POCSAG address code word format.
Fig. 7 illustrates the POCSAG synchronisation code word format.
Fig. 8 illustrates the POCSAG idle code word format.
Fig. 9 illustrates a flow diagram of the operations performed by the decoding circuit of the present invention.

Detailed Description of the Invention

Referring now to Fig. 1, a block diagram of the pager unit, including the decoding circuit, is shown. The radio pager comprises a receiver unit 10 which may be substantially identical to that of the "Metrx" radio pager which is commercially available from Motorola. Responsive to the receiver 10 is a binary detector 12, which is also responsive to a data enable signal from MPU 20 over line 11 and which transmits received data pulses to MPU 20 over line 13. MPU 20 in the preferred embodiment of the invention is an MC146805 8-bit microprocessor which is commercially available from Motorola.

Also coupled to MPU 20 are an identity ROM (read only memory) 22, a program ROM 24, and a support I.C. 26. The identity ROM 22 is programmed, using fusable links, for example, with the unique identity number of the specific pager. The identity number has two separate parts: (1) a base identity code and (2) the frame number which defines the relative position within a batch at which the frame assigned to the specific pager appears. Each pager in the pager population is assigned one of eight possible frame numbers within a batch. The identity ROM 22 is plug-interchangeable.

Each pager can respond to four different paging addresses and accordingly generates four distinguishable alerting tones. The four different paging addresses are calculated by the MPU 20 utilising the base identity code contained in the identity ROM 22, as will be described in greater detail below.

The program ROM 24 contains the computer program which controls the operation of the MPU 20 to carry out the desired decoding functions of the decoding circuit. The portion of the computer program which specifically pertains to the synchronisation mechanism of the present invention is attached hereto in source code form as Appendix A—1 through A—3.

The support I.C. 26 is a general purpose support circuit which, in the context of the present invention, performs three functions. First, it generates and regulates the secondary supply for the MPU 20, the identity ROM 22, and the program ROM 24. Secondly, it contains a timer circuit known as the "deadman timer", whose function is to reset the MPU 20 after a predetermined interval in the event that a specific instruction either is not received or remains in the instruction register for an excessive period. The function of the "deadman timer" is to prevent the decoder circuit from being held up in a lengthy software loop. Thirdly, the support I.C. 26 tests the primary power supply level on command and returns an indication of its condition.

MPU 20 generates the paging alert signals over line 27 to audio frequency amplifier 28 and ultimately transducer 30. A power supply switch 36 is responsive to an enable signal from MPU 20 over line 35. When the power supply switch 36 is enabled, the receiver power supply is connected to receiver 10 and to binary detector 12 over line 37. Battery 40 provides the primary power supply. Switch 38 is a user-operated on/off switch. Switch 32 is a "cancel" switch, the closure of which cuts short a sounding paging alert. Switch 34 is a switch used to make a selection between "normal mode" and "memory mode". In "memory mode", upon receipt of a paging request the pager does not generate the paging alert, but it stores the page request in a memory allocated for such purpose in the MPU 20. When switch 34 is switched over to the "normal mode", or when the "cancel" switch 32 is depressed at any time, any page requests stored in memory are sequentially read out and their corresponding audible alerts (each uniquely distinguishable) are generated to the pager user.

With reference now to Fig. 2, a more detailed combination block/circuit diagram of the decoder circuit is illustrated. In a preferred embodiment of the invention the MPU 20 and support I.C. 26 are mounted on an MPU and Support I.C. Board 70. The other major blocks shown in Fig. 2 are the identity ROM 22 and the program ROM 24. The identity ROM 22 is coupled to board 70 by buses 62 and 64. Bus 64 contains address lines PB4—PB7 by means of which the MPU addresses the identity ROM 22. Bus 62 comprises data lines PA1—PA5 for transmitting data from the identity ROM 22 to the MPU 20. Identity ROM 22 has its GND connection made through on/off switch 38 to the ground side of battery 40, and has its B++ terminal connected to the secondary supply line 43 from board 70.

Program ROM 24 in the preferred embodiment is an 8-by-2K bit CMOS ROM designated the MCM 65516 available from Motorola. Program ROM 24 is coupled to board 70 by secondary supply line 43 to its CS, CE, and B++ terminals; by high-order address bus 68 transmitting the high-order address bits A8—A11; by multiplexed address/data bus 66 comprising lines B0—B7 over which the low-order address bits are transmitted to program ROM 24 and data bits are transmitted from program ROM 24 to MPU 20; by address strobe line 47 to the "M" terminal of program ROM 24; by data strobe line 49 to the "G" terminal; and by ground connection over line 53 to the "GND" terminal of program ROM 24.

The MPU and Support I.C. Board 70 is illustrated in greater detail in Fig. 3, a description of which appears below. With reference still to Fig. 2, the OSC1 and OSC2 terminals of board 70 are coupled to a suitable crystal 60. The DMT terminal is connected via capacitor 58 to ground. The PB1 terminal of board 70 generates a data enable control signal to receiver 10. Terminal PA0 receives the transmitted data-in signal from the receiver 10. Terminal PB0 generates a receiver supply control signal over line 55 to the base of the transistor 42, which is turned on to provide receiver 10 with the primary supply when reception is requested by the MPU 20.

The B+ terminal of board 70 is coupled to the positive terminal of battery 40 via line 57. The COIL terminal is coupled to line 57 via coil 52. The PB2 terminal of board 70 is connected to the base of transistor switch 44 via the audio output control line 59. The PA7 terminal is coupled to one side of the "memory recall/cancel" switch 32, the other side of which is coupled to ground through line 53. The PA6 terminal of board 70 is coupled to the "memory" terminal of "memory/normal" selector switch 34, the other side of which is connected to ground through line 53. Transducer 48 provides the paging signal to the user when an audio output control signal is generated over line 59 to the base of transistor 44.

Referring now to Fig. 3, a combination block/circuit diagram of the MPU and Support I.C. Board 70 is illustrated. Since the variatious external connections between the MPU and Support I.C. Board 70 and the other pager decoder components have been previously described with regard to Fig. 2 above, only the various connections internal to the board 70 will now be discussed. The RESET terminals of MPU 20 and support I.C. 26 are inter-connected by line 61. The VDD terminal of MPU 20 is connected via line 63 to the B++ terminal of support I.C. 26. The IRQ and PA7 terminals of MPU 20 are connected to one side of pull-up resistor 80 whose other side is connected to line 63. Terminals IRQ and PA7 are also connected to line 65 which is coupled to the PA7 terminal of board 70. Pull-up resistors 81—83 and capacitor 84 also each have one side connected to line 63. Terminal PA6 of MPU 20 is connected to the other side of the resistor 81 and to line 67, which is coupled to the PA6 terminal of board 70. The PB3 terminal of MPU 20 is connected to the other side of resistor 82 and to the BATT LOW terminal of support I.C. 26. The PA0 terminal of MPU 20 is connected to the other side of the resistor 83 and to line 69 which forms the PA0 terminal of board 70. The VSS terminal of MPU 20 is coupled to the other side of capacitor 84, to the GND terminal of support I.C. 26, and to line 71 which forms the GND terminal of board 70. The TIMER and OSC2 terminals of MPU 20 are coupled together and to one side of resistor 77. The other side of resistor 77 is connected to one side of resistor 78 and to the OSC2 output terminal of board 70. The OSC1 terminal of MPU 20 is connected to the other side of the resistor 78 and to the OSC1 output terminal of board 70. The PB0—PB2 terminals of MPU 20 are each coupled respectively to one side of resistors 72, 74, and 76, and form the PB0—PB2 output terminals of board 70. Regarding the support I.C. 26, the B+ IN terminal and the B+ REG terminal are coupled together to form the B+ input terminal of board 70.

Still with reference to Fig. 3, a data strobe signal is generated at the DS terminal of MPU 20 over line 49 to the program ROM 24 to read out the appropriate data or instruction at the address specified by the address information provided to the program ROM 24 via high-order address lines A8—A11 and low-order address/data lines B0—B7. The desired data or instruction from the program ROM 24 is returned to the MPU 20 over lines B0—B7. The internal MPU data sample rate of 512 bps is obtained by using a 524.288 kHz crystal 60. The crystal output is divided by 4 in the MPU pre-scaler and is again divided by 256 by the MPU timer/counter. Thus a timer interrupt is provided every 1.95 msec, which is the appropriate bit sample period corresponding to the transmission rate of 512 bps.

Fig. 4 illustrates a block diagram of the support I.C. 26. The specific implementation of those parts of support I.C. 26 used in the present invention would be apparent to one of ordinary skill in the art. The support I.C. 26 includes a four-line decoder 90 responsive to lines PB4—PB7 from MPU 20. As was stated above, the support I.C. in the preferred embodiment is a general purpose device, and some of its operation capability is not utilised in its application to the decoding system of the present invention. For example, only a portion of the four-line decoding function is actually utilised. The four-line decoder 90 generates a CLEAR DOWN signal over line 73 to the deadman timer reset 92. The four-line decoder 90 also generates an ENABLE signal over line 75 to the battery condition test circuit 91. The deadman timer reset 92 generates a reset signal over line 86 to the MPU reset terminal, unless periodically cleared by the MPU, to prevent the MPU 20 from staying in a software loop for an excessive period of time. The battery condition test circuit 91 generates a signal over line 85 to the PB3 terminal of MPU 20 indicative of the state of the B+ primary supply. The support I.C. 26 also includes a secondary supply generator/regulator 93 which provides the secondary power supply B++ to the program ROM 24, the identity ROM 22, and the MPU 20. The B+ primary supply is provided to the secondary supply generator/regulator 93, the deadman timer reset 92, the battery condition test circuit 91, and the four-line decoder via lines 78 and 79.

Fig. 9 illustrates a flow chart of the decoding operation carried out by the decoding circuit of the present invention. In a preferred embodiment the operation which is represented by the flow chart of Fig. 9 is implemented by an MPU-controlled system, but the implementation of the decoding operation represented by Fig. 9 is not necessarily limited to such, and it is understood that the decoding operation could be performed by other means, such as a system using discrete logic or a custom I.C. A

comparison of the flow chart of Fig. 9 with the source code listing of the decoding operation given in Appendix A—1 through A—3 will indicate that various of the mnemonic designations appearing in Fig. 9 appear as macro-instructions in the software listings. For example, the GBATOK operation near the top of Fig. 9 corresponds to the GBATOK macro-instruction appearing towards the bottom of Appendix A—1.

Operation of Preferred Embodiment

The operation of the POCSAG pager decoding system will now be described with reference to the flow chart of Fig. 9. When the pager is switched on by closing switch 38, the pager battery is tested to ensure a primary supply voltage greater than a predetermined value. If the primary supply is less than the predetermined value, the MPU 20 remains in a battery check loop, and the pager unit remains inoperative.

Assuming that the primary power supply exceeds the predetermined value, the next operation is to initialise the decoding system. During the initialisation operation the 19 bit base identity code for the particular pager is read from the identity ROM 22 into MPU 20, which then calculates the 11 bit BCH parity value for each of the 4 different paging codes to which such pager is responsive. The four possible paging codes are given by the four possible bit combinations of the two function bits 20 and 21 (refer to Fig. 6). The resultant four 32 bit pager-dependent address code words are then stored in the MPU memory. Later on each of these four unique 32 bit address code words will be compared sequentially with the address code word appearing at the particular frame location assigned to this particular pager to determine whether one or two of the four possible page requests have been transmitted to this pager.

Also during initialisation the particular frame number assigned to the pager is read from the identity ROM 22 and the MPU 20 calculates (1) the time period between the end of the transmission of the synchronisation code word and the beginning of transmission of the assigned frame, and (2) the time period between the end of transmission of the assigned frame to the end of the 8-frame batch. The MPU 20 then stores these two figures into its memory. The MPU 20 also reads a threshold level number out of the identity ROM 22 and stores same for later use in the BITSYNC routine.

Referring to Fig. 9, the next operation in the flow chart is to enter the GLOBAL macro-instruction, which turns on the receiver 10. Next the GBATOK operation is performed during which the deadman timer is reset. In addition, a page alert is generated if, as a result of a previous decoding operation, a page request has been received and switch 34 has been thrown to the "normal" position.

Next the BITSYN operation is entered, in which bit synchronisation is attempted. The BITSYNC routine is performed to give a phase-lock synchronisation between the received data and the decoder circuit. It is unnecessary to encumber the present description with the details of the BITSYN operation, but in summary the MPU timer is utilised to provide a distribution, over 16 data transitions, of the positive and negative-going edges. After the 16 transitions, the distribution is examined, and if the maxima exceeds the threshold number previously read from the identity ROM 22, the MPU timer is adjusted to sample data at $\pm 1/16$th of each received data bit centre.

If bit synchronisation is achieved, the GBITOK macro-instruction is entered and an attempt is made to synchronise with the synchronisation word, as represented by the WORD SYNC operational block. If bit synchronisation is not achieved, the MPU enters the DEKONE delay routine, which turns off the power supply to the receiver and the ROM's for a period of approximately one second, representing the approximate time between batches, before bit synchronisation is re-attempted. This is a battery-saving feature.

Assuming now that the WORDSYNC operational block has been entered, the decoding circuit samples up to a maximum of 600 bits of receiver data looking for a match to the 32-bit reference synchronisation code word stored in the MPU memory. To summarise the word synchronisation comparison operation, each data sample is successively loaded into the C register of MPU 20, then rotated left from the C register into the accumulator register, the most significant bit of the accumulator register entering the least significant bit of a series of three chained 8-bit registers or memory locations. The rolling 32-bit synchronisation code word thus stored is compared during each bit sample period with the stored reference synchronisation code word, and the number of errors is calculated for each match attempt. If the number of errors after any given comparison attempt exceeds two, the routine continues, and if word synchronisation is not achieved in 600 bits, the MPU enters the battery save routine for approximately one second before re-entering the bit synchronisation routine discussed above. If any given comparison test results in an error of 2 bits or less, the MPU assumes that synchronisation with the synchronisation word has occurred, and it next proceeds to examine the contents of its assigned frame in an attempt to find one or two of its four possible unique address code words which would indicate the presence of one or two paging requests, respectively.

Before entering the routine which examines the contents of the frame for the presence of one or two address code words, a battery save routine (BATSAV1) is entered. The BATSAV1 routine switches off the receiver and ROM supply voltages until 10 msec before the expected receipt of the assigned frame, utilising the previously calculated (during initialisation) value of the time delay between the end

of transmission of the synchronisation code word and the beginning of transmission of the assigned frame information.

When the DECODE FRAME operational block is entered, the decoder circuit examines the informational content of the two address code words within the frame assigned to the particular decoder. To summarise the address code word decode operation, the received data bits corresponding to the first address code word of the assigned frame are input into the MPU C register, from which they are rotated left into the least significant bit of the accumulator register, the most significant bit of the accumulator register being input into the least significant bit of the first of a chain of three 8 bit registers or memory locations. When the entire 32 bits of the first address code word of the assigned frame have been read into the above-described memory locations, such address code word is compared sequentially to each of the four 32-bit pager-dependent address code words (previously calculated and stored during initialisation) to look for a match, indicating that the pager has received a paging request. The number of errors for each comparison is calculated, and if the number of errors is two or less, a successful match is considered to have been made, indicating the presence of a paging request. The address code word matching operation is carried out twice for each frame, since there is a provision for two address code words being contained within each assigned frame.

If a page has been received, the position of the memory/normal switch 34 is determined. If the pager is not in the memory mode of operation, the audio tone corresponding to the transmitted address code word is generated, amplified and signalled to the pager user through the transducer 48. On the other hand, if the pager is in the memory mode, the GNOPAG macro-instruction calls for storing the page request for later recall by the pager user.

Next a second battery save routine (BATSAV2) is entered, cutting the receiver power supply and reducing the decoder supply requirements during the period of time between the end of transmission of the assigned frame and the end of transmission of the batch. This again is a battery-saving feature.

The next operation (GWSCHK macro-instruction) is to check the synchronisation with the synchronisation word and to adjust the bit synchronisation if required. To summarise this operation, the synchronisation word associated with the next batch is sampled at the exact time slot in which it is expected, and it is stored in the same manner as was described above with respect to the initial synchronisation code word. The subsequent synchronisation code word is compared to the reference synchronisation code word stored in the MPU memory, and an error of two or less bits is accepted as proper word synchronisation. Assuming that word synchronisation has been achieved the second time, the decoding operation enters the BATSAV1 delay routine followed by the DECODE routine, the operation of which is as described above.

The next portion of the decoding flow chart represents a strategic, central feature of the invention. If the attempt at synchronisation with the subsequent synchronisation code word results in a error greater than two, a second attempt at such synchronisation is made, since the efficiency and sensitivity of the pager is increased if the decoding operation does not automatically revert to the bit synchronisation operation at the top of the flow chart. Because of the finite time required to carry out the bit synchronisation operation, paging information occurring within the same batch may be irretrievably lost. Thus it is desirable to assume, at least once, that the reason for failure to synchronise with the subsequent synchronisation code word may have been attributable to a noise burst or a transmission fade, for example, rather than a true out-of-synchronisation condition.

Before reattempting the word synchronisation operation, a time delay is entered, so that the receiver and decoder supply requirements are reduced until the expected transmission of the next synchronisation code word. No attempt is made to decode the contents of the intervening assigned frame, since it is not certain that word synchronisation is valid, and it would not be desirable to search for page information, since the possibility of decoding a false page indication is increased.

If on the second attempt, synchronisation to the synchronisation code word is not achieved, at least to an error of better than two bits, the operation is thrown back to the BITSYNC operational block, and bit synchronisation is attempted. Prior to attempting bit synchronisation, a delay operation is encountered, to turn off the receiver supply until about 10 msec before the next synchronisation code word is expected.

In the event that the synchronisation operation is successful regarding the subsequent synchronisation word, the bit synchronisation is re-adjusted, if necessary, utilising the mean value of a predetermined number of samples taken by the MPU timer/counter on the data transition edges of the synchronisation code word.

As mentioned above, in the event that the first attempt at synchronisation with the subsequent synchronisation code word is unsuccessful, any paging information occurring during the assigned frame of the associated batch will be ignored, so that there is some chance that paging information will be lost. However, if the second attempt at word synchronisation is successful, and the probability of success will be high, the decoding circuit will be able to immediately look at the paging information of the assigned frame in the next batch. This should be contrasted with the situation which would have occurred if the decoding operation had automatically reverted to the bit synchronisation operation after the first word synchronisation failure. In the latter case not only would possible paging information in the assigned frame associated with the current batch be lost, but in all probability the paging

information of the subsequent batch would also be lost, due to the finite time required to achieve bit synchronisation.

As a consequence, the present invention, by employing a decoding strategy which makes at least a second attempt at synchronisation with the synchronisation word reduces the chances of missing paging information. The result is a pager with higher sensitivity and increased competitiveness in the commercial area.

It will be apparent to those skilled in the art that the disclosed Pager Decoding System with Intelligent Synchronisation Circuit may be modified in numerous ways and may assume many embodiments other than the preferred form specifically set out and described above.

For example, by extension of the word synchronisation strategy discussed above, more than one re-attempt at achieving word synchronisation may be allowed. However, an excessive number of attempts at word synchronisation would result in a decreased success rate due to the possibility of (1) initial false synchronisation resulting in incorrectly timed decoding and (2) subsequent lack of synchronisation should the transmission have ended. In addition, frame decoding may be undertaken even after an unsuccessful word synchronisation operation, provided that the propability of receiving false pages is maintained at an acceptably low level.

Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

APPENDIX A—1

```
GRXON     BSET    7,TIMER
          BCLR    7,TIMCON
          BCLR    6,TIMCON
          BCLR    Ø,PORTB B+ON NO DATA ENABLE
          LDA     #$ØA
GRXOLP    WAIT
          BCLR    6,TIMCON
          DECA
          BNE     GRXOLP
          BSET    1,PORTB DATA ENABLE
          LDA     #$6
GRXOLQ    WAIT
          BCLR    6,TIMCON
          DECA
          BNE     GRXOLQ
          BSET    6,TIMCON
          RTS
GNOBIT    SICP    HI,OFF
          LDX     #HI+OFF
          STX     PORTB
          LDX     #OFF
          STX     PORTB
GNBHOP    LDX     #&242
          BSET    7,TIMER
          JSR     DEKONE
          BSET    6,TIMCON
          BRA     GBATOK

GLOBAL    BSR     GRXON     TURN ON RX.
GBATOK    SIC     HI,ON     HI I ON
          LDX     #HI+ON
          STX     PORTB

          DMTON   RESET     D.M.T.
          LDX     #$86
          STX     PORTB
          CLR     BLUM
          LDX     #$Ø6
          STX     PORTB
          JSR     BTSYNC    TRY FOR BITSYNC.
          TST     DFLAG     TEST FOR PAGE
          BEQ     GBITNP
          BRCLR   6,PORTA,GBITNP PAGE IF IN NORMAL
          JSR     PCALL
```

APPENDIX A—2

```
        GBITNP  BRCLR   Ø,BFLAG,GNOBIT IF NO BIT SYNC RE
        GBITOK  DMTON   OTHERWISE RESET DMT
                LDX     #$86
                STX     PORTB
                CLR     BLUM
                LDX     #$Ø6
                STX     PORTB
                JSR     WDSYN1 TRY FOR WORDSYNC.
                SIC     DMT,ON
                LDX     #DMT+ON
                STX     PORTB
                CLR     BLUM
                SICP    HI,ON
                LDX     #HI+ON
                STX     PORTB
                LDX     #ON
                STX     PORTB
                BRCLR   4,BFLAG,GNOWD1
        GWDOK1  JSR     BTSAV1 OTHERWISE WAIT
                JSR     DECODE THEN DECODE FRAME
                DMTON   AND             RESET D.M.T.
                LDX     #$86
                STX     PORTB
                CLR     BLUM
                LDX     #$Ø6
                STX     PORTB
                JSR     DECODE          AND THEN IF CALL
                TST     DFLAG           RECEIVED GO TO
                BEQ     GNOPAG          PCALL, OTHERWISE
                BRCLR   6,PORTA,GNOPAG  WAIT AGAIN UNTIL
                SICP    HI,ON
                LDX     #HI+ON
                STX     PORTB
                LDX     #ON
                STX     PORTB
                JSR     PCALL           SYNC. WORD IS
        GNOPAG  JSR     BTSAV2          EXPECTED.
                SICP    HI,ON
                LDX     #HI+ON
                STX     PORTB
                LDX     #ON
                STX     PORTB
        GWSCHK  JSR     WDSYN2          CHECK WORD SYNC. &
                SICP    HI,ON
                LDX     #HI+ON
                STX     PORTB
                LDX     #ON

                STX     PORTB
                BRCLR   4,BFLAG,GNOWD2  ADJUST BIT SYNC.I
```

APPENDIX A—3

```
        GWDOK2  BCLR    Ø,GFLAG1        OTHERWISE, CHECK THE
                BRA     GWDOK1          TO WAIT FOR NEXT FRAME.
        GNOWD1  WAIT
                BCLR    6,TIMCON
                DMTOFF
                LDX     #$85
                STX     PORTB
                CLR     BLUM
                LDX     #$Ø5
                STX     PORTB
                WAIT
                BCLR    6,TIMCON
```

Appendix A—3 (contd.)

```
        LDX     #&242
        JSR     DEKONE
        BSET    6,TIMCON
        JMP     GBATOK
GNOWD2  WAIT
        BCLR    6,TIMCON
        DMTOFF
        LDX     #$85
        STX     PORTB
        CLR     BLUM
        LDX     #$Ø5
        STX     PORTB
        WAIT
        BCLR    6,TIMCON
        BRCLR   Ø,GFLAG1,GNWHOP
        BCLR    Ø,GFLAG1
        LDX     #&246
        JSR     DEKONE
        BSET    6,TIMCON
        JMP     GBATOK
GNWHOP  BSET    Ø,GFLAG1
        LDX     #&249
        JSR     DEKONE
        DMTON
        LDX     #$86
        STX     PORTB
        CLR     BLUM
        LDX     #$Ø6
        STX     PORTB
        BRA     GWSCHK
```

Claims

1. A decoding system for use with a receiver receiving a transmission signal comprising a periodically recurring synchronisation code word and at least one address code word, said decoding system comprising:

means for receiving said synchronisation code word;

means for comparing a received synchronisation code word with a reference code word and for generating an indication of the quality of such comparison;

means for generating a comparison count representative of the number of successive comparisons of successively received synchronisation code words with said reference code word;

decisional means responsive to said quality indication and to said comparison count, said decisional means generating a first signal if the quality of a received synchronisation code word exceeds a predetermined threshold value, generating a second signal if the quality of the received synchronisation code word does not exceed a pre-determined threshold value and a pre-determined number of comparison counts has not been exceeded, and generating a third signal if the quality of the received synchronisation code word does not exceed said pre-determined threshold value and said pre-determined number of comparison counts has been exceeded.

2. The decoding system recited in Claim 1, wherein said system further comprises:

means for synchronising said decoding system to bit transitions in said transmitted signal;

means responsive to said third signal for actuating said bit synchronisation means; and

means for actuating said synchronisation code word comparing means when bit synchronisation is achieved.

3. The decoding system as recited in Claim 2 and further comprising:

means for receiving said at least one address code word;

means responsive to said at least one address code word for comparing said address code word to a reference address code word;

means for generating an indication of a match when said address code word matches said reference address code word; and

means for actuating said address code word comparing means in response to said first signal and for inhibiting the operation of said address code word comparing means in response to said second and third signals.

4. The decoding system recited in Claim 3 and further comprising:

means responsive to said third signal for enabling the operation of said bit synchronisation means and for inhibiting the operation of said synchronisation code word comparing means.

5. The decoding system recited in Claim 4, wherein said at least one address code word occurs during a pre-determined time interval in said transmission signal with respect to the synchronisation code word, and further comprising:

means for determining a first time period corresponding to the time between the end of said synchronisation code word and the beginning of said time interval and for determining a second time period corresponding to the time between the end of said time interval and the beginning of a subsequent synchronisation code word;

a power supply for enabling operation of said decoding system; and

means responsive to said determining means for disabling the power supply to said receiving means during said first and second periods.

6. In a decoding system for use with a receiver receiving a transmission signal comprising a periodically recurring synchronisation code word and at least one address code word, said decoding system including means for receiving said synchronisation code word, the improvement comprising

means for comparing a received synchronisation code word with a reference code word and for generating an indication of the quality of such comparison;

means for generating a comparison count representative of the number of successive comparisons of successively received synchronisation code words with said reference code word; and

decisional means responsive to said quality indication and to said comparison count, said decisional means generating a first signal if the quality of a received synchronisation code word exceeds a predetermined threshold value, generating a second signal if the quality of the received synchronisation code word does not exceed a pre-determined threshold value and a pre-determined number of comparison counts has not been exceeded, and generating a third signal if the quality of the received synchronisation code word does not exceed said pre-determined threshold value and said pre-determined number of comparison counts has been exceeded.

7. A radio paging device for decoding a transmission signal comprising a plurality of digitally encoded bits including a periodically recurring synchronisation code word and at least one address code word representing a page request, said device comprising:

receiver means; and

synchronisation and decoding means including:

a microprocessor responsive to said receiver means;

memory means coupled to said microprocessor and containing instructions and data for use by said microprocessor;

means for synchronising the operation of said synchronisation and decoding means to said transmitted bits;

means for comparing a received synchronisation code word with a reference code word stored in said memory means and for generating a first indication of a match condition;

means responsive to said first match indication for comparing said at least one address code word with at least one reference address code word stored in said memory means and generating a second indication of a match condition; and

means responsive to said second match indication for indicating a transmitted page request.

8. A method of operating a decoding system decoding a transmission signal comprising a plurality of digitally encoded bits including a periodically recurring synchronisation code word and at least one address code word, said method comprising:

1) synchronising the operation of said decoding system to said transmitted bits;

2) synchronising the operation of said decoding system to a first one of said synchronisation code words;

3) comparing said at least one address word with at least one reference address code word and indicating a match condition if they are substantially similar;

4) making a determination of whether said decoding system is synchronized to a second one of said synchronisation code words;

5) making a subsequent determination of whether said decoding system is synchronised to a third one of said synchronisation code words, if said decoding system was determined not to have been in synchronisation with said second synchronisation code word;

6) returning to step (1) if said decoding system was determined not to have been in synchronisation with said third one of said synchronisation code words; and

7) returning to step (3) if said decoding system was determined to have been in synchronisation with said third one of said synchronisation code words.

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